

Fig. 1 (Prior Art)

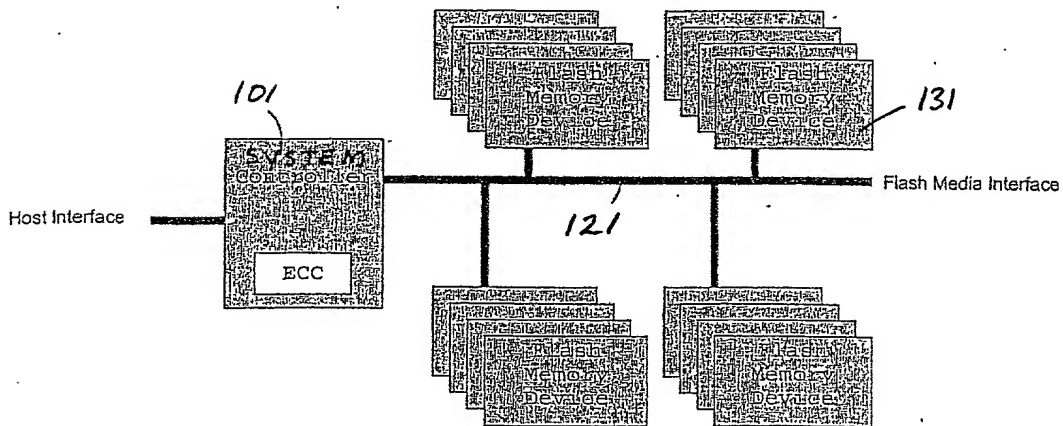


Fig. 2 (Prior Art)

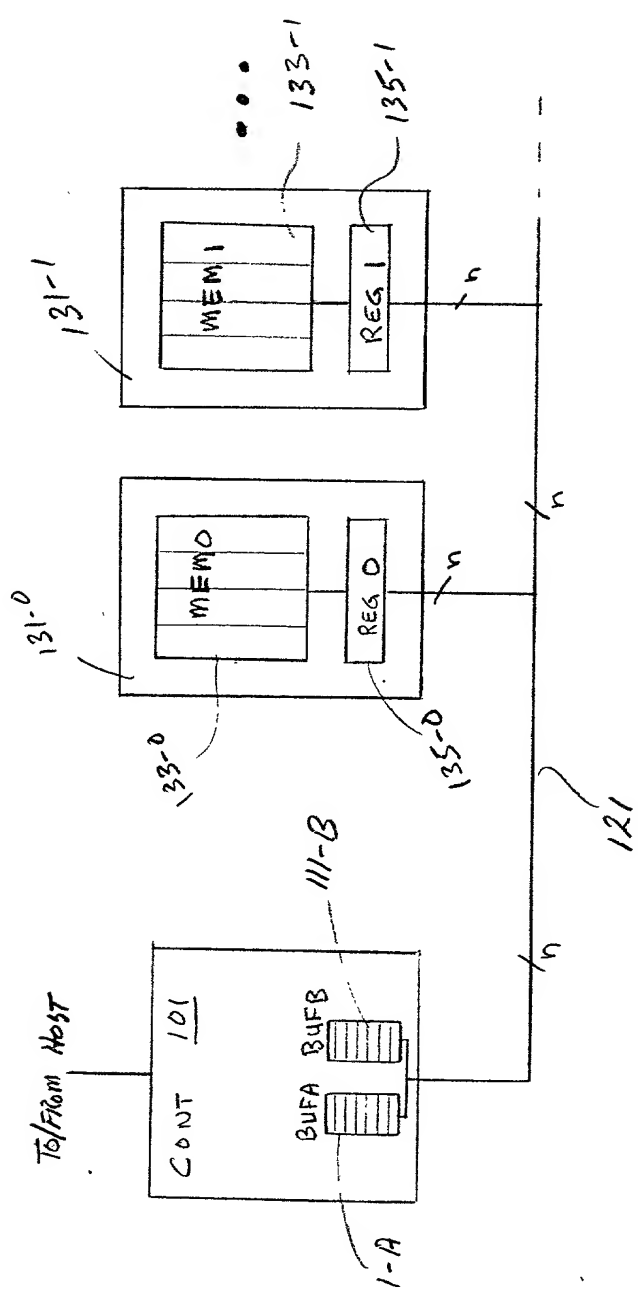


Figure 3

Controller

Buffer A Transfers  
(host to controller)

Sect 1	Sect 2	Sect 3	Sect 4
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Buffer B Transfers  
(host to controller)

Sect 5	Sect 6	Sect 7	Sect 8
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Memory 0

Data Transfers  
(controller to memory)

Program Operations  
(in memory)

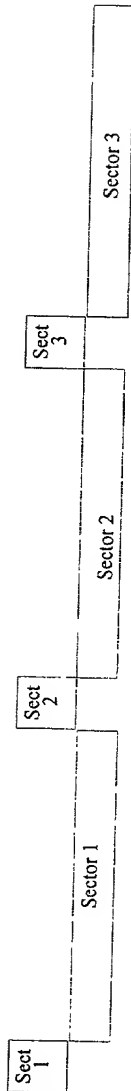


Figure 4A

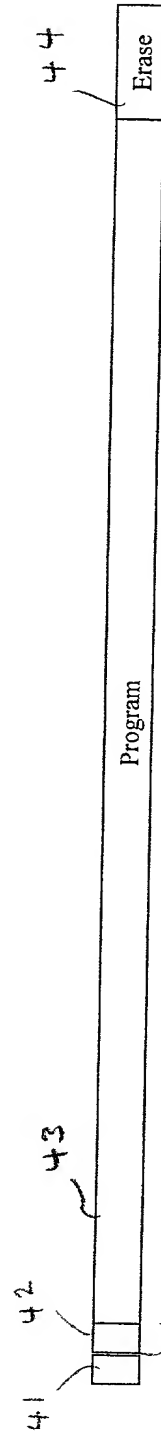


Figure 4B

# Controller

Buffer A Transfers  
(host to controller)

Sect	Sect	Sect	Sect
1	2	3	4

Buffer B Transfers  
(host to controller)

Sect	Sect	Sect	Sect
5	6	7	8

## Memory 0

(controller to memory)  
Data Transfer

Sect	Sect	Sect	Sect
1	2	3	4

Program Operations  
(in memory)

Sector 1
Sector 2
Sector 3
Sector 4

Sect	Sect	Sect	Sect
5	6	7	8

Sector 5
Sector 6
Sector 7
Sector 8

Sect	Sect	Sect	Sect
9	10	11	12

Figure 5B

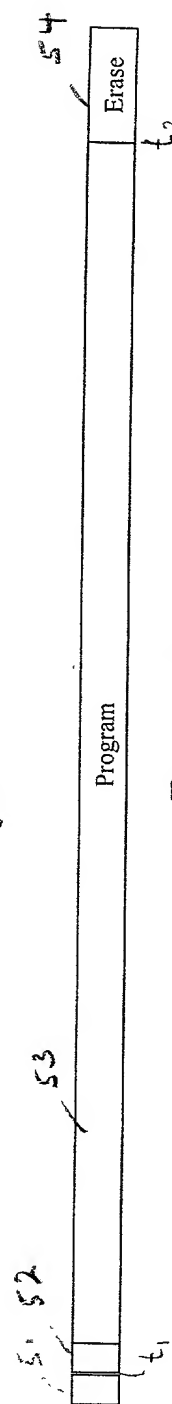
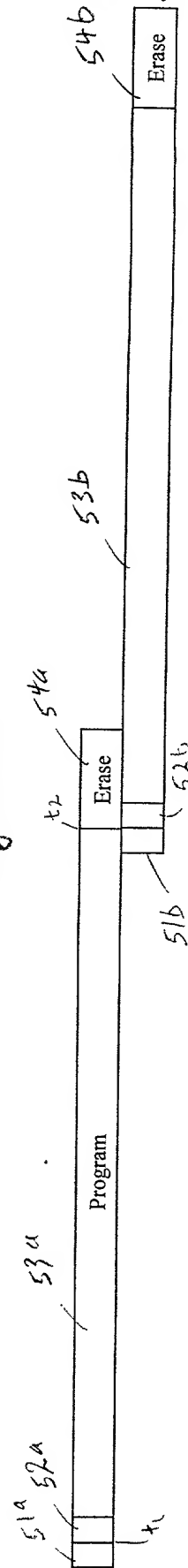


Figure 5C



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Page 4 of 6

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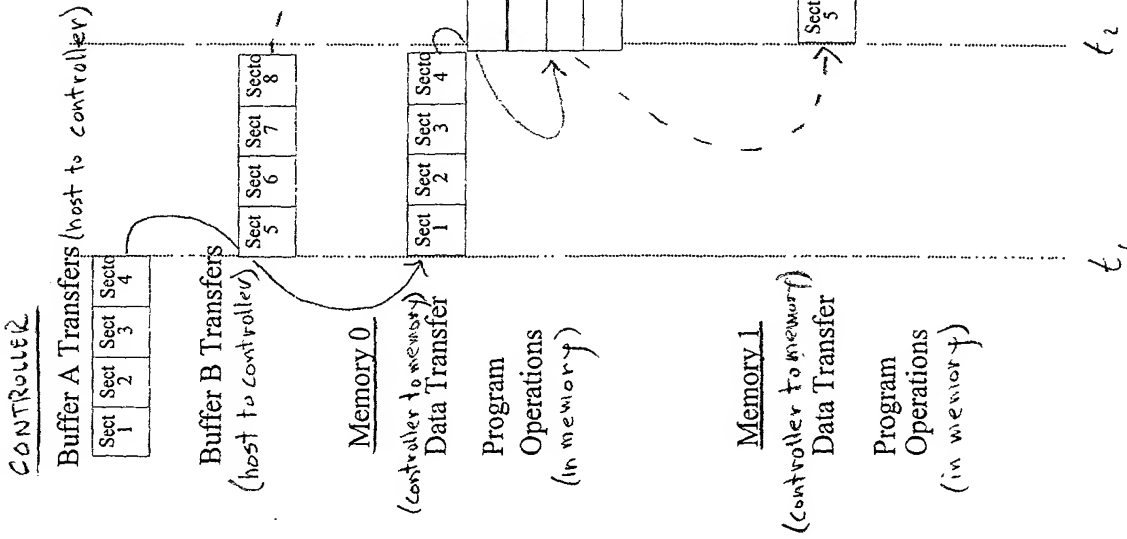


Figure 4A

